

Abstract of the Disclosure

A time delay compensation circuit comprises delay cells having various unit time delays. A delay-locked loop, a type of the time delay compensation circuit, includes a phase detector, a delay line, and a filter unit. The phase detector compares the phase of the external clock signal with that of the feedback clock signal and outputs a phase difference as an error control signal. The delay line includes a plurality of delay cells having various unit time delays. The number of delay cells is adjusted in response to a predetermined shift signal. The delay line receives the external clock signal and outputs an output clock signal, which is obtained by controlling the phase of the external clock signal. The filter unit generates the shift signal, which selects the number of delay cells in the delay line, in response to the error control signal. In the time delay compensation circuit, the front delay cells, which are used to compensate for a delay of an external clock signal having a high frequency, have short unit time delays so as to reduce jitter due to quantization error. Also, the rear delay cells, which are used to compensate for a delay of the external clock signal having a low frequency, have long unit time delays so as to reduce the number of delay cells required for the delay compensation.